Mars: A 64-core ARMv8 Processor

Charles Zhang
Phytium Technology Co., Ltd
Statements

The following slides are presented to introduce the general features of one of our products, instead of any commitment about it. It is for information purposes only, and may not be incorporated into any contract. It is not suggested to make purchasing decisions accordingly. The development, release, and timing of any features or functionality described here remains at the sole discretion of Phytium.
A Brief Introduction of Phytium

- China corporation, founded in 2012
  - Guangzhou
  - Tianjin

Vision
- Leading edge CPU and ASIC provider in China

Market focuses on chips for
- Internet & Cloud Computing infrastructure
- Traditional workload mainframe servers
## China is a Fast-growing Server Market

<table>
<thead>
<tr>
<th>Company</th>
<th>1Q15 Revenue</th>
<th>1Q15 Market Share (%)</th>
<th>1Q14 Revenue</th>
<th>1Q14 Market Share (%)</th>
<th>1Q15-1Q14 Growth (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inspur</td>
<td>332,613,480</td>
<td>21</td>
<td>227,328,256</td>
<td>17</td>
<td>46</td>
</tr>
<tr>
<td>Dell</td>
<td>322,063,140</td>
<td>20</td>
<td>246,281,271</td>
<td>19</td>
<td>31</td>
</tr>
<tr>
<td>Lenovo</td>
<td>295,914,571</td>
<td>18</td>
<td>80,084,826</td>
<td>6</td>
<td>270</td>
</tr>
<tr>
<td>HP</td>
<td>217,487,450</td>
<td>14</td>
<td>167,775,923</td>
<td>13</td>
<td>30</td>
</tr>
<tr>
<td>Huawei</td>
<td>197,490,419</td>
<td>12</td>
<td>189,963,266</td>
<td>14</td>
<td>4</td>
</tr>
<tr>
<td>Sugon</td>
<td>140,377,091</td>
<td>9</td>
<td>70,705,366</td>
<td>5</td>
<td>99</td>
</tr>
<tr>
<td>Others</td>
<td>104,566,737</td>
<td>6</td>
<td>329,549,621</td>
<td>25</td>
<td>-68</td>
</tr>
<tr>
<td>Total</td>
<td>1,610,512,888</td>
<td>100.0</td>
<td>1,311,688,529</td>
<td>100.0</td>
<td>23</td>
</tr>
</tbody>
</table>

**Source:** Gartner (May 2015)

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<th>1Q14 Market Share (%)</th>
<th>1Q15-1Q14 Growth (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HP</td>
<td>3,191,694,948</td>
<td>23.8</td>
<td>2,890,992,229</td>
<td>25.5</td>
<td>10.4</td>
</tr>
<tr>
<td>Dell</td>
<td>2,296,473,026</td>
<td>17.1</td>
<td>2,006,639,006</td>
<td>17.7</td>
<td>14.4</td>
</tr>
<tr>
<td>IBM</td>
<td>1,887,939,141</td>
<td>14.1</td>
<td>2,244,631,789</td>
<td>19.8</td>
<td>-15.9</td>
</tr>
<tr>
<td>Lenovo</td>
<td>970,254,659</td>
<td>7.2</td>
<td>127,973,470</td>
<td>1.1</td>
<td>658.2</td>
</tr>
<tr>
<td>Cisco</td>
<td>890,179,930</td>
<td>6.6</td>
<td>616,620,000</td>
<td>5.4</td>
<td>44.4</td>
</tr>
<tr>
<td>Others</td>
<td>4,157,871,704</td>
<td>31.0</td>
<td>3,469,383,444</td>
<td>30.6</td>
<td>19.8</td>
</tr>
<tr>
<td>Total</td>
<td>13,394,413,409</td>
<td>100.0</td>
<td>11,356,239,939</td>
<td>100.0</td>
<td>17.9</td>
</tr>
</tbody>
</table>

**Source:** Gartner (May 2015)
What is Mars for?

- High performance
- High volume of memory
- High bandwidth memory access
- High bandwidth I/O access
- Large scale cache coherency maintained

- Moderate performance
- High power efficiency
- High density computing
- High bandwidth memory access
- Low cost

Source: IT Candor, April 2010
Mars Overview

- **Architecture Features**
  - 64 Xiaomi cores, ARMv8 compatible
  - Hardware-maintained global cache coherency
  - Panel-based data affinity architecture
  - Mesh topology on chip network
  - 32MB L2 cache
  - 8 Cache & Memory Chips (CMC)
    - 128MB L3 cache
    - 16 DDR3-1600 channels
  - Two 16-lane PCIE3.0 i/f
  - ECC and parity protection on all caches, tags and TLBs

### Physical
- ~180M instances
- 2.0GHz@28nm
- 120W

### Performance
- Peak: 512GFLOPS
- Mem BW: 204GB/s
- I/O BW: 32GB/s
Panel Architecture

- Eight Xiaomi Cores
  - Compatible design with ARMv8 arch license
  - Both AArch32 and AArch64 modes
  - EL0~EL3 supported
  - ASIMD-128 supported
  - Adv. hybrid Branch Prediction
  - 4 fetch/4 decode/4 dispatch Out-of-Order superscalar pipeline

- Cache Hierarchy
  - Separated L1 ICache and L1 Dcache
  - Shared L2 cache, totally 4MB
  - Directory-based cache coherency maintenance
    - Directory Control Unit (DCU)

- Routing Cell
Xiaomi Core

- BTB
- DirPre
- IndPre
- SRS
- Arch. Reg file
- Phy. Reg file
- ITLB
- I Cache
- Instruction Buffer
- Decoder
- Decoder
- Decoder
- Decoder
- Rename Logic
- Dispatch Logic
- Reorder Buffer
- L2 Cache
- Loop Detect
- STB & Prefetch
- Debug/Trace/Interrupt/Timer
- LD/ST Queue
- DTLB
- D Cache
- Integer Queue
- FP/VT Queue
- FP/SIMD Queue
- FP/SIMD Queue
- ALU/BR
- ALU/SIMD
- ALU/SIMD
- ALU/SIMD

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Xiaomi Core Front End

- 32KB L1 instr. Cache
- Next line prefetch
- Hybrid Branch Predictor
  - 2048-entry BTB
  - Direction predict with TAGE predictor
  - 512-entry indirect predictor
  - 48-entry Speculative Return Stack
- Four instructions fetched per cycle
- 32-entry instruction buffer
- Loop detect and Instr. Cache bypass
Xiaomi Core Decode, Rename & Dispatch

- Up to four instructions decoded per cycle
- 192 physical registers
- Up to four instructions renamed per cycle

- Up to four instructions dispatched per cycle
- Reorder buffer can hold 160 instructions, and about 210+ instructions can be in-flight in the whole pipeline.
- Dispatch in-order, execution out-of-order, retirement in-order.
Xiaomi Core Function Units

- Four separated 16-entry integer queues
  - One integer unit can process both multi-cycle integer instructions and branch instructions
  - The other three integer units can only process single-cycle integer instructions
- One shared 16-entry floating point and ASIMD queue
  - Two FP/ASIMD units equipped, which can be combined into one lockstep ASIMD unit.
  - FMA supported in both units.
  - FMUL: 3 cycles, FADD: 3 cycles, FMA: 6 cycles
Xiaomi Core Function Units

• One 24-entry load/store queue
• 32KB L1 data cache
  • 6 outstanding loads
  • 4 cycles latency from load to use
• Next line and stride detected data prefetch
• Streamlined pattern auto detected
Cache coherence protocol

- Hawk cache coherence protocol
  - Distributed directory-based global cache coherency
  - MOESI-like packet-based coherence protocol
  - A home node DCU (directory control unit) supports
    - Affinitive pairing of L2Cs and CMCs
    - “Infinite” capacity for non-conflicting Reads & Writes
    - Optimized transaction flow for exclusive atomic accesses
    - Reduced latency by cacheline forwarding
Network on Chip

- 2D Concentrated Mesh Architecture
  - Cell based switch with 6 bidirectional ports
  - Uniform package format for each port, a port can be configured to be connected with a device or cascade cell
  - 4 physical channels for CC and 1 channel for debug, DOR Y-X routing
  - Low latency: 3 cycles for each hop
  - High bandwidth: 384GB/s each cell

<table>
<thead>
<tr>
<th>Dest.</th>
<th>Lat. (cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>9</td>
</tr>
<tr>
<td>3</td>
<td>12</td>
</tr>
<tr>
<td>4</td>
<td>15</td>
</tr>
<tr>
<td>5</td>
<td>12</td>
</tr>
<tr>
<td>6</td>
<td>9</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>Avg.</td>
<td>9</td>
</tr>
</tbody>
</table>
Cache & Memory Chip

- L3 cache
  - 16MB Data Array
  - 2MB Data ECC
- DDR bandwidth
  - 2 x DDR3-800: 25.6GB/s
- Proprietary interface between Mars & CMC
  - Parallel interface
    - Needs more pins, but lower latency than serdes
  - Separate write/cmd and read data channel
    - Effective read channel bandwidth: 12.8GB/s
    - Effective write/cmd channel bandwidth: 6.4GB/s
Latency of affinitive access

<table>
<thead>
<tr>
<th>Memory access</th>
<th>latency(ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Local L1 cache hit</td>
<td>~2</td>
</tr>
<tr>
<td>Local L2 cache hit</td>
<td>~8</td>
</tr>
<tr>
<td>Affinitive L2 cache hit</td>
<td>~20</td>
</tr>
<tr>
<td>Affinitive L3 cache hit</td>
<td>~36</td>
</tr>
<tr>
<td>Affinitive DDR access</td>
<td>~70</td>
</tr>
</tbody>
</table>

- Panel : 2.0GHz
- NoC: 2.0GHz
- CMC: 1.5GHz

* PCB latency not considered
Memory Tune (mTune)

- Rich Data Collection
  - Number of cache hits/misses for L1/L2/L3
  - Workload of cache pipelines
  - Busyness of the NoC
  - ECC corrections of the memory system

- Support Multiple Metrics
  - Average Miss rate/Hit rate
  - Minimal/Maximal/Average Access Latency
  - Bandwidth Analysis
  - Concurrent Average Memory Access Time (CAMAT)

- Support MPI/OpenMP Applications
  - Thread behavior analysis
  - Inter-process behavior analysis
Scalable Debug System

- ARMv8 CoreSight Compatible debug system
- Scalable dedicated debug network across 64 cores
- Distributed debug components
- Configurable events broadcast scope
- Timestamp broadcasts with single signal to simplify implementation
Physical Design

- 28nm process
- 0.9v core/1.8v IO
- 10 metal layers
- ~180M instances
- 2.0GHz
- 120W
- 640mm² die size
- FCBGA
- ~3000 pins
Performance Evaluation

- SpecCPU2006

**SPEC_CPU2006_base**

- INT: 19.2
- FP: 17.8

**SPEC_CPU2006_rate**

- INT: 672
- FP: 585

Single copy of SPEC CPU benchmark

64 copies of SPEC CPU benchmark
Performance Evaluation

- STREAM

STREAM triad

- Bandwidth (GB/s)
- #cores
Next Generation Scale-up CPU

- More powerful core
  - Aggressive Branch Predictor
  - Multithreading
  - More aggressive ILP exploitation
  - Wider SIMD
- More RAS features
- Higher bandwidth memory access
- Higher power efficiency
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